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BT-6/M-19 36010

VHDL AND DIGITAL DESIGN

ECE-304E

Opt. (ii)

Time : Three Hours] [Maximum Marks : 100

Note : Attempt *Five* questions in all, selecting at least *one* question from each Unit. All questions carry equal marks.

Unit I

1. (a) Write a note on "Why use VHDL ?". **10**
   (b) Differentiate between PLDs and CPLDs. **10**

2. (a) Describe the design synthesis using VHDL. **10**
   (b) Design 3-bit synchronous counter using 22V10 PLDs. **10**

Unit II

3. (a) Differentiate between variable and signal assignment statements. **10**
   (b) Using structural modeling, write the VHDL code for 1-bit full adder using only NAND gates. **10**

4. (a) Explain the signal drivers in detail. **10**
   (b) In data flow modeling, differentiate between concurrent and sequential signal assignments. **10**

Unit III

5. (a) Define and explain the use of generics in entity and component declarations. **10**
   (b) Differentiate between functions and procedures. **10**

6. (a) Why configurations are used ? Explain in detail. **10**
   (b) Show that use of package declaration and package body in a VHDL program. **10**

Unit IV

7. (a) Define and explain "Aliases". **10**
   (b) Describe "User Defined Attributes". **10**

8. (a) Dexplain the if-generation scheme. **10**
   (b) With the help of examples, explain predefined attributes. **10**