(2)

Roll No.

8717

Printed Pages: 3

BT-7/M 12

VLSI DESIGN

Paper-ECE-401-E

Time allowed: 3 hours]

[Maximum marks: 100

Note: Attempt any five questions, selecting at least one from each unit.

Unit-I

- (a) Describe with Illustrations, the two-metal n-well CMOS fabrication process to show how a CMOS inverter is fabricated. List all the masks in sequence of usage.
 - (b) Discuss the voltage transfer characteristics of E/D NMOS inverter.
- 2. (a) Derive the drain current equation for a MOS transistor. What is channel length modulation?
 - (b) Draw the stick diagram of a 1-bit full adder in E/D NMOS technology.

Unit-II

- (a) Why do we get progation delays? For the CMOS fabrication process with device parameters as: μ_a.C_{ox} = 120 μA/V², μ_p.C_{ox} = 40 μA/V², μ_p.C_{ox} = 40 μA/V², μ_p.C_{ox} = 40 μA/V², μ_p.C_{ox} = 0.8 V, V_{TO,F} = -1.0 V, V_{pp} = 3 V, W_{min} = 1.2 μm. Design a CMOS inverter by determining the channel widths W_n and W_p of the nMOS and pMOS transistors, to meet the propagation delay times τ_{pin} ≤ 0.2 ns and τ_{pin} ≤ 0.15 ns. Assuming the output load capacitance of 0.2 pF and ideal step input. 10
 - (b) What is packaging? Discuss various packaging technologies.
- 4. Comparing the two scaling theories, constant-E and constant-V, show analytically by using equations how the delay time, power dissipation, power density, power-speed product are affected in terms of the scaling factor S. Which theory is more suitable for smaller geometries?

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Unit-III

5.	What do you understand by routing? Discuss	the
	various routing algorithms. What is the grid mode	el for
	global routing? http://www.kuonline.in	20

Discuss the various Partitioning Algorithms. Discuss
the advantages and disadvantages of each.

Unit-IV

- 7. Describe the delay models in Physical Design. How are timing constraints applied?
 20
- 8. Write short notes on :
 - (a) Delay models in physical design. 10
 - (b) Timing minimization. 10