Roll No. ..... Total Pages : 04

BT-3/D-19 33133

DIGITAL ELECTRONICS
ES-207A

Time : Three Hours] [Maximum Marks : 75

Note : All questions in Part A and Part B are compulsory. Attempt any *four* questions from Part C, selecting *one* question from each Unit.

Part A

1. Answer the following questions : 5×3=15
   (i) Explain the conversion of AND operation into OR operation with the help of deMorgan theorem.
   (ii) Explain conversion of standard form into canonical form.
   (iii) Explain designing and working of half adder.
   (iv) State the difference between positive edge triggering, negative edge triggering and level triggering of flip-flops.
   (v) List the specifications of D/A converters.

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Part B

Note : Attempt all questions.

2. Perform the following operations : 5
   (i) $(27)_7 + (53)_2$
   (ii) $(34\text{-}48)_2$ using 2's compliment.
   Simplify (A+B)(A'+C) to minimum number of literals.

3. Explain the different properties of logic families. Explain the working of TTL NAND gate. 5

4. Explain the working of JK flip-flop. What is race around condition in JK flip-flop ? How it can be solved by master slave flip-flop ? 5

5. Draw the basic circuit of a ROM cell. Explain its working. 5

Part C

Note : Attempt *one* question from each Unit.

Unit I

6. Using Q-M method, obtain the minimal expression for F = $\sum$m(6, 7, 8, 9, 13, 15) + d(10, 11, 12, 14). Also realize the expression using NAND gate only. 10

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7. Reduce the following expression using K-Map : **10**

   (a) $F = \Pi M(1, 2, 5, 6, 8, 9, 10)$

   (b) $f = \Sigma(0, 1, 4, 7, 13, 14) + d(5, 8, 15)$

   Realise the obtained expression using NAND/NOR logic.

Unit II

8. (a) State and explain the working of BCD adder with its logic diagram. **6**

   (b) Design a 3 to 8 decoder. **4**

9. What do you mean by multiplexer ? Explain the working of n:1 mux. Design a multiplexer tree f 32:1 mux using 8:1 and 2:1 mux. **10**

Unit III

10. (a) Draw a diagram for 5 bit ring counter using JK flip-flop. Explain its working with the help of timing diagram. **10**

    (b) Design a synchronous mode-6 counter. Use JK flip-flop for designing the counter. **10**

11. (a) What do you mean by Register ? Draw and explain the logic diagram of serial in serial out shift right register. **10**

    (b) Explain how JK flip-flop can be converted into D flip-flop. **10**

Unit IV

12. What are the different types of memories ? Explain them. **10**

13. What do you mean by PLD ? Discuss different types of PLD. Implement the following Boolean functions using PLA : **10**

    $F1(A,B,C) = \Sigma m(1, 2, 4, 6)$, $f2\ (A, B, C) = \Sigma m(0, 1, 5, 7)$, $f3\ (A, B, C) = \Sigma m(1, 2, 3, 5, 7)$