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GSE/M-20 **1493**

ELECTRONICS–I

(Electronic Devices and Circuits-II)

Paper–I

Time : Three Hours] [Maximum Marks : 40

Note : Attempt *five* questions in all, selecting *one* question from each unit. Question No. 1 is compulsory.

Compulsory Question

1. (a) How a FET can be used as a voltage-variable resistance ?

(b) What is the condition for thermal stability ?

(c) What is the need of coupling in a multistage amplifier ?

(d) What is thermal runaway ? How is it related to the biasing of a transistor ? (2×4=8)

UNIT–I

2. (a) Show that the stability factor for the collector to base bias is $s = \dfrac{(1+\beta)}{\left[1+\dfrac{\beta R_c}{R_B + R_c}\right]}$ and $s' = \dfrac{-\beta.s}{(1+\beta)(R_B + R_c)}$.

5

(b) Explain why biasing is necessary in an amplifier ? 3

3. (a) For the collector to base bias circuit, the BJT used is specified to have β values in the range of 20 to 200. If feedback resistance is 100 kΩ and emitter resistance is 1 kΩ, for the two extreme values of β(20 & 200), find V_E, I_E and V_B. 4

(b) The operating point is required to be selected in the middle of load line in an amplifier circuit. Why ? What are the reasons due to which Q-point gets shifted ? Explain. 4

UNIT–II

4. (a) A 50-NPN transistor is used in self-bias CE amplifier, having β = 50 at room temperature. The circuit has R_1 = 90 kΩ and R_2 = 10 kΩ and R_E = 1.5 kΩ. The values of other components are adjusted to have the collector current I_C = 2 mA. Calculate the values of s, s', s''. 5

(b) Why thermal runaway cannot take place, if $V_{CE} < \frac{V_{CC}}{2}$. 3

5. (a) Draw a self-bias circuit. Explain qualitatively why such a circuit is an improvement on the fixed bias circuit, as for as stability is concerned. How is the load line drawn for a self-bias circuit ? 4

(b) The mid frequency gain of a RC coupled amplifier is 100. The values of higher and lower cut off frequencies are 100 kHz and 100 H_Z, respectively. Find the frequency at which the gain reduces to 80. 4

UNIT–III

6. (a) The *h*-parameters of the transistors used in two stage RC coupled amplifier are h_{fe} = 400, h_{ie} = 8 kΩ. If the shunt capacitance at high frequency is 500 pf, coupling capacitance is 0.5 μF and R_L = 15 kΩ, calculate the lower and higher cut off frequencies of the amplifier. The source may assume to be negligibly small. 5

(b) Outline the general method for obtaining the high frequency response of two interacting amplifier stages. 3

7. (a) Sketch the response of an amplifier to a low frequency square wave. What is tilt and how is it related to the low 3–dB frequency f_L ? 4

(b) For an RC coupled amplifier, the mid frequency gain is 200. If the gain falls by 6 dB at the lower cut off frequency, calculate the gain at the cut-off frequency in dB. 4

UNIT–IV

8. (a) If two identical FET, are connected in parallel then prove that the effective transconductance is doubled and drain resistance is halved. The amplification factor remains unchanged. 4

(b) A common source amplifier uses FET having γ_d = 10 kΩ and μ = 16. Calculate the voltage and output resistance of the amplifier for load resistance equal to (i) 100 kΩ (ii) 200 kΩ (iii) 1 MΩ. 4

9. (a) A common source FET amplifier uses load resistance R_L = 100 kΩ and an unbypassed resistance R_s connected between source and ground. The γ_d of FET is 200 kΩ and g_m = 0.1 mΩ^{-1}. Compute the voltage gain and output resistance of the amplifier for R_s equal to : (i) 5 kΩ (ii) 50 kΩ (iii) 20 kΩ. 4

(b) Draw the small signal model of a FET and show that the FET behaves as a voltage controlled current source (VCCS). 4