Roll No. ..... Total Pages : 3

GSM/M-20 **1634**

ELECTRONIC

(Digital Electronic–II)

Paper–II

Time Allowed : 3 Hours] [Maximum Marks : 40

Note : Attempt **five** questions in all, selecting at least **one** question from each Unit. Question No. **1** is compulsory. All questions carry equal marks.

Compulsory Question

1. (a) What is Buffer register ? Write its use. 2

   (b) How does PLA differ from a PROM ? 2

   (c) Define the following terms of DAC

   (i) Accuracy

   (ii) Resolution. 2

   (d) What are the applications of DMA transfer of Data in Computer system ? 2

UNIT–I

2. (a) Explain the working of 4-bit serial-in serial-out register. 4

   (b) Design and draw the circuit of a shift register to generate some sequence. 4

3. (a) With the help of circuit diagram explain the working of 4-bit bi-directional shift register. 4

(b) Discuss the working of parallel-in-parallel-out register. 4

UNIT–II

4. (a) Explain magnetic core memory in detail. 4

(b) What is the difference between Static and Dynamic RAMs ? Write their advantages and disadvantages. 4

5. (a) What are Read Only Memories ? Explain using logic diagram, how a matrix of diodes is connected to form a ROM. 4

(b) Explain the working of bipolar RAM cells with the help of circuit diagram. 4

UNIT–III

6. (a) Discuss the Weighted Resistor type digital-to-analog converter (DAC). Find the general expression for the output voltage of this D/A converter. 5

(b) Calculate the value of LSB, MSB and Full-scale output for an 8-bit DAC for 0-10V range. 3

7. (a) Name different methods of A/D conversion and explain the principle of dual slope integration A/D convertor. Also show that the accuracy of conversion is independent of the clock frequency drift. 5

   (b) Find out how many bits A/D converter is required to achieve a resolution of 1mV if the maximum full scale input voltage is 10 volts. 3

UNIT–IV

8. What do you understand by DMA mode of data transfer ? Explain the working of DMA controller with block diagram. 8

9. How the input-output devices can be interfaced through programmed I/O technique ? Explain, how the waiting time of CPU can be reduced in programmed I/O. 8