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Printed Pages : 2

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BT-6 / M-18

DIGITAL DESIGN USING VERILOG

Paper–ECE-304 N

Time allowed : 3 hours] *[Maximum marks : 100*

Note : *Attempt any **five** questions by selecting atleast **one** question from each unit.*

Unit–I

1. (a) Explain ASIC Design flow in detail. 7

2. Explain the following terms.

   (i) $ monitor

   (ii) Nets

   (iii) Ternary operator

   (iv) Memory declaration

   (v) Net Data type 15

Unit–II

3. (a) Design 4:16 decoder circuit using 3:8 decoder and also write its verilog code using gate level modeling. 10

   (b) Explain tri-state gates with its instantiation syntax. 5

4. (a) Explain initial construct and wait construct with syntax. 5

   (b) Design 4-bit left shift register and also write its verilog code using behavioural modeling. 10

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Unit–III

5. (a) Define unary and relational operators. 7

   (b) Explain BCD adder and write its verilog code using dataflow modeling. 8

6. (a) Explain switch primitives with their syntax in verilog. 8

   (b) Design three input NAND gate using resistive pullup load. 7

Unit–IV

7. (a) Explain User-defined primitives and write a UDP for 2-input NAND gate. 7

   (b) Explain system tasks and functions. 8

8. (a) Explain compiler directives. 8

   (b) Write a verilog code for 8-bit parity check by calling a function for odd parity. 7

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