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**BT-6 / M-18**

**VHDLAND DIGITAL DESIGN**

**Paper–ECE–304 E Opt.-I**

*Time allowed : 3 hours*

*[Maximum marks : 100*

*Note:- Attempt five questions in all, selecting at least one from each unit.*

**Unit-I**

- 1. (a) Write a note on "Design synthesis using VHDL". 10
- (b) Describe the architecture and features of FPGAs. 10
- 2. (a) Write a note on "Why use VHDL?". 10
- (b) Draw Macrocell and explain the timing parameters of 22V10 PLD. 10

**Unit-II**

- 3. (a) Using examples, differentiate between if and case statements. 10
- (b) Explain the concept of multiple drivers in the concurrent signal assignments. 10
- 4. (a) Differentiate between inertial and transport delay models.
- (b) Describe use of block statements in VHDL. 10

**Unit-III**

- 5. (a) Define and explain the use of generics in configuration. 10
- (b) Describe use clause using example. 10

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- 6. (a) Write a note on architecture configurations. 10
- (b) Draw and explain a typical compilation process using design file and design libraries. 10

**Unit-IV**

- 7. (a) Describe the for-generation scheme. 10
- (b) Explain "Type Conversions". 10
- 8. (a) Define and explain the "Qualified Expressions". 10
- (b) Explain "Guarded Signals". 10

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