

18/05/17

Roll No.

Printed Pages : 2

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BT-6 / M-17
VHDL & DIGITAL DESIGN
Paper-ECE-304E, Opt. I

Time allowed : 3 hours]

[Maximum marks : 100

Note : Attempt five questions in all, selecting at least one question from each unit.

Unit-I

1. (a) Design Full Adder circuit using PLA. 10
(b) Differentiate between FPGAs and CPLDs. 10
2. (a) What is a Programmable logic device ? Explain 22V10 architecture. 10
(b) Explain the major capabilities of VHDL. 10

Unit-II

3. (a) With suitable example, explain signal drivers. 10
(b) Write a VHDL code for a synchronous decade counter using J-K flip-flops. 10
4. (a) Write a VHDL code for 8:1 Multiplexer using case statement. 10
(b) Explain block statement with suitable example. 10

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Unit-III

5. (a) Explain component configuration in detail. 10
(b) Differentiate between functions and procedures. 10
6. (a) Write a VHDL code to find largest of three integers using functions in architecture. 10
(b) Explain Generics with suitable example. 10

Unit-IV

7. (a) Write a VHDL code for 2-bit full adder using generate statement. 10
(b) Explain Alias using suitable examples. 10
8. (a) Describe Qualified expressions. 10
(b) Explain user defined attributes. 10

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