Roll No. ..... **Total Pages : 03**

BT-7/M-20 **37015**

ADVANCED MICROPROCESSORS

ECE-423E/EE-423E

Time : Three Hours] [Maximum Marks : 100

Note : Attempt *Five* questions in all, selecting at least *one* question from each Unit.

Unit I

1. (a) Define memory segmentation concept for 32-bit microprocessors. Explain in detail the segmentation scheme used in protected mode for IA-32 architecture processors. **10**

(b) With the help of a suitable diagram explain in detail the functioning of all the visible registers present in X86 families of processors ? **10**

2. (a) Explain in detail the different operating modes of X86 families of processors and also show the transaction among various modes with the help of a suitable diagram. **10**

(b) Explain in detail the concept of pipelining in Pentium processor. Support your answer with a suitable diagram and explain the different stages of pipelining in Pentium processor. **10**

Unit II

3. (a) Draw the internal architecture of 80486 microprocessor and explain its functioning in detail. **15**

(b) Draw the flag register for x86 processor and explain the functioning of each bit. **5**

4. (a) Explain the functioning of different pins of 80286 Processor. **10**

(b) Draw and explain the system segment descriptors used in 80286 processor. **10**

Unit III

5. (a) Draw the internal architecture of Pentium-II processor and explain the functioning in detail. **10**

(b) Draw the internal architecture of the mathematical co-processor for 80286 and also explain the register set of the co-processor. **10**

6. (a) Draw the internal architecture of 80287 co-processor and also draw the register set for the same processor. **10**

(b) Explain the task management concept for P-6 family of processors. **10**

Unit IV

7. (a) Draw the internal architecture of 80387 microprocessor and explain the function of each block in detail. **10**

(b) Explain the register set of 80487 co-processor. **10**

8. Explain the following :

(a) Protection Mechanism **5**

(b) Branch Prediction **5**

(c) Assembler Directives. **5**

(d) x87 Transcendental Instructions, Load Constants Instructions. **5**