Roll No. ..... **Total Pages : 02**

BT-7/M-20 **37140**

DIGITAL VLSI DESIGN

ECE-425N

Time : Three Hours] [Maximum Marks : 75

Note : Attempt *Five* questions in all, selecting at least *one* question from each Unit.

Unit I

1. Describe the following in MOS devices : **15**

(a) Body Effect

(b) Noise Margin

(c) Latch-up.

2. Describe in detail the fabrication process for MOS device. **15**

Unit II

3. Draw the diagram of MOS inverter and explain its working. **15**

4. Explain the switching characteristics of MOS inverter. What are the considerations in deciding the size of devices ? **15**

Unit III

5. Explain the working of 2-input NAND gate using depletion type MOS loads and also derive expression for V_{OH} and V_{OL}. **15**

6. Write short notes on the following : **15**

(a) Pass Transistors

(b) Primitive logic gates

(c) Complex logic gates.

Unit IV

7. Discuss the following : **15**

(a) Edge-triggered flip-flop

(b) D latch

(c) SR latch.

8. Describe CMOS implementation of D-latch with the help of timing diagram. **15**