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BT–7 / M–14

VLSI DESIGN

Paper – ECE-401 E (Opt. ii)

Time allowed : 3 hours] *[Maximum marks : 100*

Note : *Attempt any five questions by selecting at least one question from each unit. Each question carries equal marks.*

Unit–I

1. (a) Explain the processing steps in fabrication of NMOS technology with neat sketches.

   (b) Explain about stick diagram with colour coding and monochrome encoding.

2. (a) Draw the circuit of CMOS Inverter and explain its operation.

   (b) What are the various pull-up transistors used for inverters?

Unit–II

3. Write down the difference between CMOS and Bi-CMOS technology.

4. What is latch-up problem ? How latch up problem is solved in P-well, N-well CMOS process ?

Unit–III

5. Explain Kernighan-Lin partitioning algorithm with an example.

6. Explain Fiduccia-Mattheyses partitioning algorithm with an example.

Unit–IV

7. What are the various delay models used in VLSI design. Explain RC delay model in detail.

8. What do you mean by via ? Explain how via minimization is done ?