Roll No. ..... Total Pages : 2

BT-7/DX **8711**

VLSI DESIGN

Paper : ECE-401(E)

Time : Three Hours] [Maximum Marks : 100

Note : Attempt any *five* questions by selecting at least *one* question from each unit.

UNIT–I

1. (a) Draw and discuss Voltage transfer characteristics of a CMOS inverter and mark all the critical voltages. How do they get modified for a resistive-load inverter ? 14

   (b) For a resistive load inverter circuit with V_{DD} = 5 V, Process transconductance $k_n = 20\mu A/V^2$, $V_{T0} = 0.8$ V, $R_L = 200$ kΩ and W/L = 2. Calculate the logic threshold voltage of the circuit. 6

2. Describe the basic fabrication sequence of E/D NMOS LOCOS process using labelled illustrations. How many masks are required to fabricate an inverter in such a process ? List them in sequence of usage. 20

UNIT–II

3. (a) Implement the XOR using logic function block using (i) Transistor level circuit, and (ii) Symbolic layout. 10

(b) For a CMOS inverter with $V_{T0,n} = 1.0$ V, $V_{T0,p} = -1.2$ V, $\mu_n C_{ox} = 45\ \mu A/V^2$, $\mu_p C_{ox} = 25\mu A/V^2$, $V_{DD} = 5$ V, $(W/L)_n = 10$, $(W/L)p = 20$, and the output load capacitance of 1.5 pF, calculate the rise time of the output signal using exact method. Assume input to be ideal rectangular pulse switching between 0 V and 5 V. 10

4. What is Combined Scaling theory ? How do various performance parameters scale in it ? How can it be extended to other scaling theories ? Also discuss the limits to scaling. 20

UNIT–III

5. (a) What is Global Routing ? Write a note on routing in FPGAs. 10

   (b) What is Partitioning ? Why is it important ? 10

6. Discuss hierarchically defined floorplan. What is the concept of simulated annealing ? Name and discuss the performance parameters associated with floorplanning. 20

UNIT–IV

7. What do you understand by Timing-driven placement and routing ? Explain briefly. 20

8. Write short notes on :

   (a) Performance issues in Layouts. 10

   (b) Power minimization. 10