

Roll No.

Total Pages : 02

BT-7/M-20 37032

VHDL AND DIGITAL DESIGN

EE-415E

Time : Three Hours]

[Maximum Marks : 100

Note : Attempt *Five* questions in all, selecting at least *one* question from each Unit.

Unit I

- 1.** Discuss the various capabilities of VHDL in design.
Describe in detail various design units of VHDL. **20**
- 2.** Discuss basic architecture and features of FPGA. List various application of FPGA in today's world. **20**

Unit II

- 3.** Write a VHDL program for 4 : 1 Multiplexor using behavioural modeling. **20**
- 4.** Discuss in detail structural modeling in VHDL using example of XOR Gate. **20**

Unit III

5. Why we use configuration in VHDL ? Discuss configuration declaration using suitable example. **20**
6. What is packaging in VHDL ? Discuss package declaration and package body using suitable examples. **20**

Unit IV

7. Discuss for generation scheme in VHDL to generate 4 bit full adder. **20**
8. Discuss various attributes in VHDL. **20**